



MAIL STOP  
AMENDMENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: T. Haze Attorney Docket No.: LEPA122745

Application No.: 10/823,297 Art Unit: 2822 / Confirmation No.: 4560

Filed: April 13, 2004 Examiner: P.E. Perkins

Title: METHOD OF FORMING BUMP PAD OF FLIP CHIP  
AND STRUCTURE THEREOF

RESPONSE TRANSMITTAL LETTER

Seattle, Washington 98101  
June 28, 2006

TO THE COMMISSIONER FOR PATENTS:

A. Response Transmittal

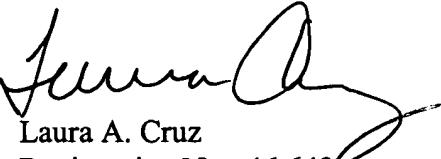
Transmitted herewith is a response to an Office Action in the above-identified application. No additional claim fee is required.

B. Additional Fee Charges or Credit for Overpayment

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16, 1.17 and 1.18 which may be required during the entire pendency of the application, or credit any overpayment, to Deposit Account No. 03-1740. This authorization also hereby includes a request for any extensions of time of the appropriate length required upon the filing of any reply during the entire prosecution of this application.

Respectfully submitted,

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Date: June 28, 2006  
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RESPONSE

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TO THE COMMISSIONER FOR PATENTS:

This paper is filed in response to the Office Action mailed on March 28, 2006. Currently, Claims 1-9 are pending in the application. Of these, Claims 7-9 are withdrawn from consideration as being drawn to a nonelected invention. Claims 1-6 have been examined and stand rejected.

The Rejection of Claims 1, 2, 4, and 5 Under 35 U.S.C. § 103(a)

Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (KR 1020030072855), in view of Cobley et al. (U.S. Patent No. 6,736,954).

*A prima facie* rejection requires a suggestion or motivation, either in the references or in the knowledge generally available to combine references or to modify a reference, a reasonable expectation of success, and all the claim limitations must be taught or suggested in the prior art.

In rejecting the claims, the Examiner states that:

Lee et al. disclose a method of forming a bump pad of a flip chip including subjecting a surface of an insulating layer to electroless copper plating to prepare electroless copper plating layer, which is then coated with photosensitive material; exposing to light and developing the photosensitive material to prepare a resist pattern, which is then pulse plated to form a pulse plating layer; a; and removing the resist pattern

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prepared at the second step and the electroless copper plating layer prepared at the first step (constitution).

Lee et al. do not disclose subjecting the pulsing plating layer to electrolytic copper plating using direct current, to prepare a direct current plating layer.

Cobley et al. disclose a method of forming a bump pad of a flip chip including a subjecting a surface of an insulating layer to electroless copper plating to prepare electroless copper plating layer and subjecting the pulse plating layer to electrolytic copper plating using direct current, to prepare a direct current plating layer (col. 5, lines 29-38; col. 11, lines 42-63).

... Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lee et al. by subjecting the pulsing plating layer to electrolytic copper plating using direct current, to prepare a direct current plating layer as taught by Cobley et al. to improve the physical-mechanical properties of the plated layer (col. 13, lines 9-35).

#### The Prior Art References Do Not Teach All Claim Limitations

Claim 1 includes a sequence of steps, comprising an electroless copper plating step, exposing and developing a photosensitive material to prepare a resist pattern, pulse plating a first layer, plating using direct current to form a second layer, and removing the resist pattern and the electroless copper plating layer.

Lee et al. describes the sequence of electroless copper plating, exposing and developing a dry film, and a second copper plating step (which is not described as a pulse plating step) to form a lead wire for interconnecting the circuit and the solder ball land, followed by a stripping step for removing the dry film.

Even assuming for the sake of argument that Lee et al. describes a pulse plating layer after developing the photosensitive material, Lee et al. teaches a stripping step follows the plating step, not a second electrolytic copper plating step using direct current, as claimed. Therefore, Lee et al. does not disclose two plating processes for forming the bump pad.

While the Office Action recognizes that Lee et al. does not disclose copper plating using direct current, the Office Action states that Cobley et al. discloses a method of forming a bump pad of a flip chip, including subjecting a surface of an insulating layer to electroless copper plating to prepare the electroless copper plating layer and subjecting the pulse plating layer to electrolytic copper plating using direct current. As support for this, the Office Action cites Col. 5, Lines 29-38, and Col. 11, Lines 42-63.

However, Cobley et al. does not teach pulse plating followed by direct current plating; Lee et al. does not teach or suggest two plating steps. Even if direct current plating or pulse plating can be substituted for the plating step of Lee et al., the references still fail to teach or suggest using pulse plating to form a first layer followed by DC plating to form a second layer.

There is no Suggestion or Motivation to Combine or Modify References

The Examiner states "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lee et al. by subjecting the pulsing plating layer to electrolytic copper plating using direct current, to prepare a direct current plating layer as taught by Cobley et al. to improve the physical-mechanical properties of the plated layer (col. 13, lines 9-35)." However, this characterization of Cobley et al. is inaccurate. A *prima facie* rejection requires a suggestion or motivation from either the references or the generally available knowledge, which is not based on applicant's disclosure.

Cobley teaches at Col. 13, lines 9-13.

By preventing or substantially reducing the amount of additive breakdown, the additive consumption inhibiting compounds provide for improved brightness of plated metal and improved physical-mechanical properties of the plated metal.

Therefore, Cobley et al. does not teach that pulse plating followed by DC plating improves physical-mechanical properties. Cobley et al. teaches that the improved physical-mechanical properties are improved by preventing or substantially reducing the amount of additive

breakdown by using the inhibiting compounds in plating baths as taught by Cobley et al. The purpose of Cobley et al. is to teach a novel metal plating bath and method of plating a metal on a substrate where the metal plating bath contains heteroatom organic compounds that prevent or inhibit the consumption of metal plating bath additives. (See the Abstract.) Accordingly, the *prima facie* rejection is not tenable, since there is no suggestion or motivation.

Furthermore, the instant specification teaches at page 8, line 21, and at page 25, line 21, that a direct current plating layer following a pulse plating layer results in a solder bump that is high in density and has improved reliability. Therefore, the Examiner cannot look to applicant's disclosure for the suggestion or motivation.

Accordingly, the withdrawal of the rejection is respectfully requested.

The Rejection of Claims 3 and 6 Under 35 U.S.C. § 103(a)

Claims 3 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al., in view of Cobley et al., as applied to Claim 1 above, and further in view of Wang et al. (U.S. Patent No. 5,519,177).

In rejecting Claims 3 and 6, the Examiner states:

Lee et al. in view of Cobley et al. disclose the subject matter claimed above except the photosensitive material coated plating layer being 20  $\mu\text{m}$  thick and wherein the pulse plating layer is 5-10  $\mu\text{m}$  thick.

Wang et al. disclose a method of forming a bump pad of a flip chip including a first step of subjecting a surface of an insulating layer (2) to electroless copper plating to prepare electroless copper plating layer, which is then coated with photosensitive material (3); a second step of exposing to light and developing the photosensitive material to prepare a resist pattern, which is then pulse plated to form a pulse plating layer (Fig. 1c-1f; col. 14, lines 45-67).

Referring to claims 3 and 6, Wang et al. disclose the photosensitive layer and plating layer of claim 1 wherein the photosensitive layer may be 20  $\mu\text{m}$  thick and the plating layer may be 25  $\mu\text{m}$  thick (col. 14, lines 45-67). It is noted that the specification contains no disclosure of

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either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to form the photosensitive layer as 20  $\mu\text{m}$  thick and the pulse plating layer as 5-10  $\mu\text{m}$  thick since it has been held that "in such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

In rejecting Claims 3 and 6, the Examiner stated that Wang et al. disclosed a method of forming a bump pad of a flip chip. However, neither "bump pad" or "flip chip" appear in the disclosure of Wang et al.

In rejecting Claims 3 and 6, the Examiner also states that Wang et al. discloses subjecting a surface of insulating layer 2 to electroless copper plating to prepare electroless copper plating layer, which is then coated with photosensitive material 3. As support for this, the Examiner refers to Col. 14, lines 45-67, and Figures 1c-1f. Applicant respectfully disagrees with this characterization of Wang et al. Figures 1c-1f describe an insulating substrate 1, being coated with an adhesive 2. The surface of the adhesive is then roughened. A palladium catalyst is applied onto the substrate provided with the roughened adhesive layer. A plating resist 3 is formed on the roughened surface of the adhesive (see Figure 1e). An electroless copper plated layer is then formed in spaces of the plating resist 3 on top of the adhesive layer 2 (see Figure 1f).

Therefore, the reference does not teach or suggest an electroless copper plating layer, which is then coated with photosensitive material. The reference teaches applying the resist 3 before electroless copper plating.

The reference also does not teach pulse plating to form a pulse plating layer. The reference teaches electroless copper plating after forming the resist.

In rejecting the claims, the Examiner states that the photosensitive layer of Wang et al. may be 20  $\mu\text{m}$  thick. The reference does not teach this either. The Examiner has stated that the

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photosensitive layer is element numbered 3. The reference teaches that adhesive layer 2 has a thickness of 20  $\mu\text{m}$  (Col. 14, line 51).

It is clear by the above statement that the Examiner now equates the adhesive layer 2 of the Wang et al. reference with the photosensitive material of Claim 1. This statement is inconsistent with the earlier statement that the photosensitive material is element numbered 3.

The comparison made of the photosensitive material of Claim 1, which is exposed to light and developed, and thereafter removed, compared to the adhesive 2 of Wang et al. is not appropriate. It is apparent by reading the disclosures of the instant application and the Wang et al. patent that the resist of Claim 1 and the adhesive 2 of Wang et al. are not similar. In Claim 1, the resist is a solder resist that allows the electroless copper plating layer to form within spaces in the resist (see Fig. 3c of the instant application). The resist of Claim 1 is subsequently removed (see Fig. 3e of the instant application). In contrast, the adhesive layer 2 of the Wang et al. patent is applied directly on the insulating substrate 1 so that a subsequent electroless copper plating method results in formation of copper plating directly on the adhesive layer 2, not the insulating layer 1 (see Fig. 1f of the Wang et al. patent).

Although the thickness of the plating layer taught by Wang et al. falls outside of the range in Claim 6, the Examiner nevertheless states that Claim 6 is obvious and cites *In re Woodruff* for the proposition that "in such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range."

Section 2144.05, Part I, of the M.P.E.P. at p. 2100-148 (rev. 3, August 2005), states "[i]n the case where the claimed ranges 'overlap or lie inside ranges disclosed by the prior art' a *prima facie* case of obviousness exists." *In re Wertheim*, 541 F.2d 257, 191 U.S.P.Q. 90 (C.C.P.A. 1976); *In re Woodruff*, 919 F.2d 1575, 16 U.S.P.Q.2d 1934 (Fed. Cir. 1990) (The prior art taught

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carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5% allowed for concentrations slightly above 5%, thus the ranges overlapped.").

Claim 6 recites a pulse plating layer of 5-10  $\mu\text{m}$  thick, whereas Wang et al. teaches electroless copper plating layer 4 having a thickness of 25  $\mu\text{m}$ . Therefore, the ranges do not overlap.

The Examiner states that it is the burden of the applicant to show that the particular claimed range is critical. However, this applies where there is a *prima facie* case of obviousness based on overlapping ranges. (See M.P.E.P. § 2144.05 III., p. 2100-149, rev. 3, August 2005).

Because there is no overlap of ranges, there is no *prima facie* case of obviousness, and applicant needs not show unexpected results.

Accordingly, the withdrawal of the rejection is respectfully requested.

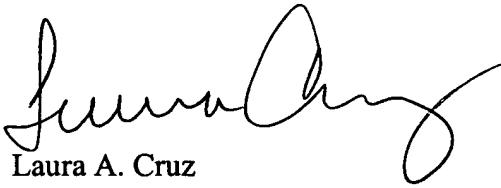
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CONCLUSION

In view of the foregoing remarks, applicant respectfully submits that Claims 1-6 are allowable. If the Examiner has any further questions or comments, the Examiner may contact the applicant's attorney at the number provided below.

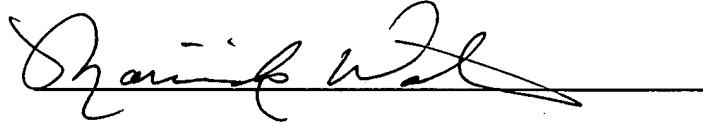
Respectfully submitted,

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